WENJI FANG

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EDUCATION

Hong Kong University of Science and Technology (Guangzhou) 2022 – Present

M.Phil. in Microelectronics, supervised by Prof. Hongce Zhang and Prof. Zhiyao Xie
Core Grade: 4.13/4.3

Nanjing University of Aeronautics and Astronautics 2017 – 2021

B.Eng. in Electrical Engineering and Automation
Core Grade: 4.0/5.0 (90/100)

WORK EXPERIENCE

Hong Kong University of Science and Technology (Guangzhou) Dec. 2021 – Jul. 2022

Research Assistant Advisor: Prof. Hongce Zhang

Formal property verification of microprocessors

Peng Cheng National Laboratory Jul. 2021 – Dec. 2021

Digital IC Physical Design Intern Advisor: Dr. Biwei Xie

Back-end physical design of an SoC from RTL to GDSII layout

NOTABLE PROJECTS

Register-Transfer Level (RTL) Design Quality Prediction

Dec. 2022 – Present

- Extracted abstract syntax tree of RTL as graph representation
- Collected ground truth PPA data with commercial EDA tools
- Developed suitable machine learning model for timing, power, area prediction separately
- Published a first-authored paper in *ICCAD'23*

Symbolic-Simulation-Guided Invariant Synthesis for Microprocessor Verification

Dec. 2021 – Nov. 2022

- Achieved an end-to-end unbounded formal verification framework for microprocessors
- Constructed a symbolic simulation framework to get the abstract states of the microprocessor
- Generated the inductive invariants to implement the unbounded checking of the safety properties
- Tested the framework with multiple pipelined processor cases
- Published a first-authored paper in *TACAS'23*, and participated in a journal paper published in *TCAD'23*

"One Student One Chip" Project

Jul. 2021 – Dec. 2021

- Responsible for physical design of an SoC with commercial EDA tools, which has been taped out based on 110nm SMIC technology node
- Completed an entire back-end flow, including *Logic Synthesis, Static Timing Analysis, Formal Equivalence Checking, Place & Route, and Physical Verification*
- Connected with SoC team to jointly complete clock specification and standard design constraints
- Realized RTL design of a single-cycle RISC-V processor

Real time Visible Spectrum Analysis Chip System (Undergraduate Final Year Project)
Nov. 2020 – Jun. 2021

- Designed a spectrometer silicon photonics integrated circuit technology to sample the spectral signals, which has been taped out based on 180nm CUMEC technology node
- Recovered the unknown input spectral signals with machine learning methods, such as linear regression and compressed sensing
- Applied for two national invention patents, and participated in a journal paper published in *PhotoniX'23*

PUBLICATIONS

Wenji Fang, Yao Lu, Shang Liu, Qijun Zhang, Ceyu Xu, Lisa Wu Wills, Hongce Zhang, and Zhiyao Xie, "MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design". *International Conference on Computer Aided Design (ICCAD)*, 2023.
Wenji Fang, Guangyu Hu, and Hongce Zhang, "r-map: Relating Implementation and pecification in Hardware Refinement Checking". *IEEE Transactions on Computer Aided Design of Integrated Circuits and systems (TCAD)*, 2023.
Wenji Fang, and Hongce Zhang, "WASIM: A Word-level Abstract Symbolic Simulation Framework for Hardware Formal Verification". *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, 2023.

HONORS AND AWARDS

ICCAD Student Scholar Program	2023
3rd Place Award of EDAthon Contest	2023
Full Postgraduate Scholarship, HKUST(GZ)	2022-2024
Infineon Technology Scholarship	2020
Finalist Prize of the Mathematical Contest in Modeling and Interdisciplinary Contest in Modeling	2020
1st Prize of the Electronics Circuit Design Competition of NUAA	2019
Outstanding Volunteer, 2019 Youth Science Camp (Jiangsu Camp)	2019
Academic Scholarship, NUAA	2017-2021

SKILLS

- Languages
  English (IELTS 7.0), Chinese (Native)
- Electronics Software
  Cadence and Synopsys EDA tools, Xilinx Vivado, Yosys
- Programming Language
  Python, C/C++, Verilog, MATLAB