DAC Young Fellows

THE CHIPS TO SYSTEMS CONFERENCE 62

NetTAG: A Multimodal RTL-and-Layout-Aligned Netlist Foundation Model via Text-Attributed Graph

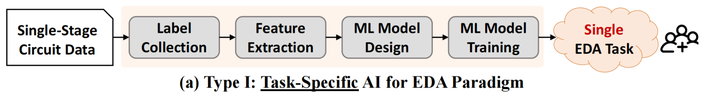
Wenji Fang, Wenkai Li, Shang Liu, Yao Lu, Hongce Zhang, Zhiyao Xie

Hong Kong University of Science and Technology

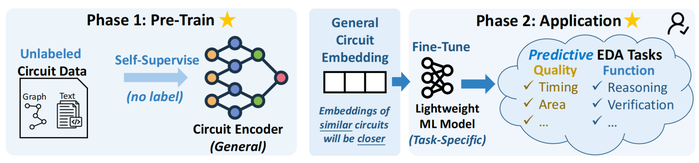
Background: Circuit Foundation Model

❑ Paradigm Shift of AI for EDA

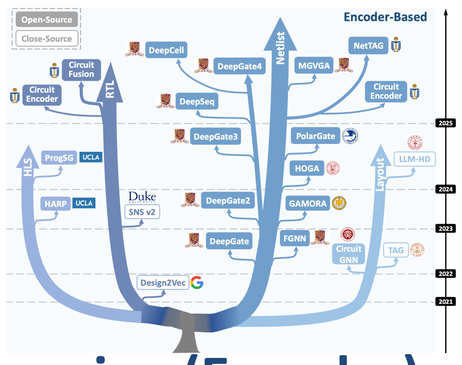
- **Widely adopted:** task-specific supervised learning
- **New trend:** general self-supervised Circuit Foundation Model



(a) Type I: Task-Specific AI for EDA Paradigm

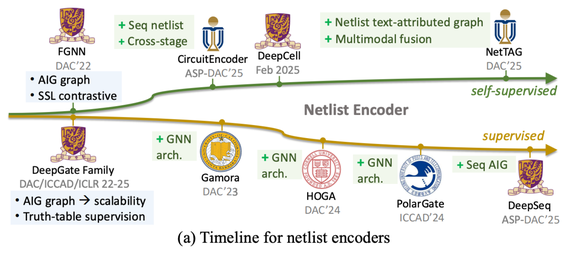


(b) Type II: General Encoder-Based Circuit Foundation Model Paradigm



❑ Netlist Representation Learning (Encoder)

- Most actively explored type of circuit encoders
- **Limitation:** graph-only for AIG
  - Structure over function
  - Need functional supervision
  - No physical encoding, PPA?

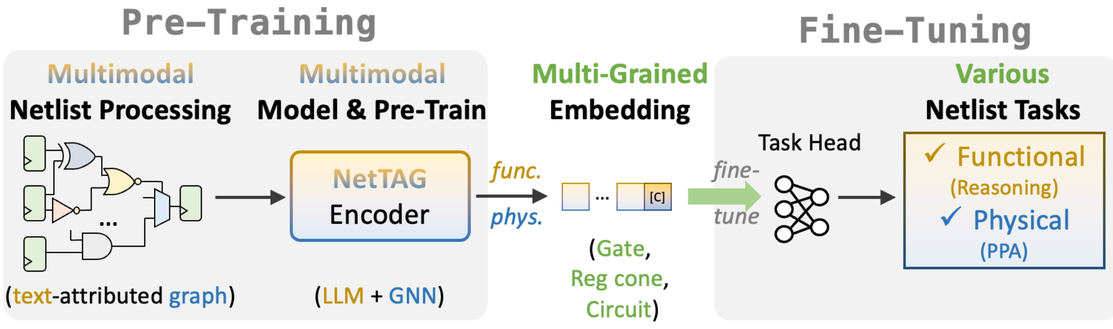


(a) Timeline for netlist encoders

Method: Multimodal Netlist Encoder

❑ NetTAG Overview

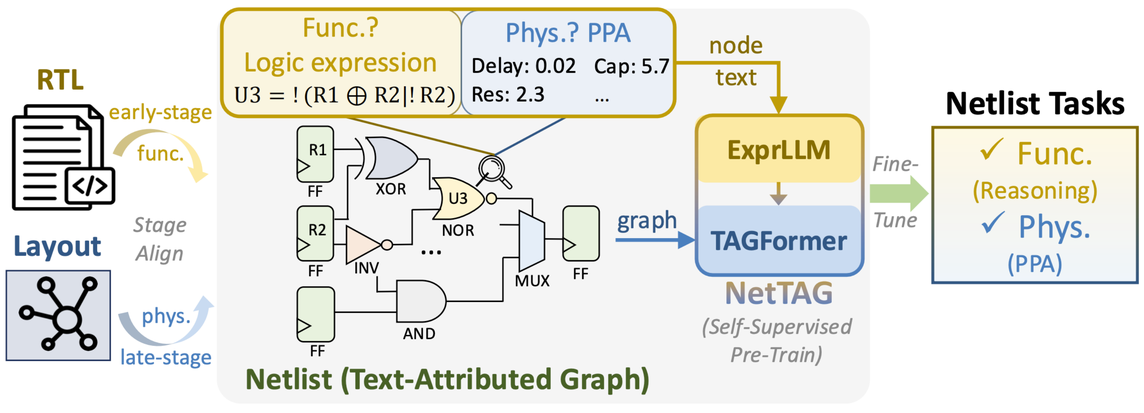
- **Key idea:** fuse local gate text with global structure graph via TAG
- **Key advantages:**
  - Any gate type & multi circuit granularities & func. + phys. tasks



- **Key steps:** netlist preprocess → pre-training → fine-tuning

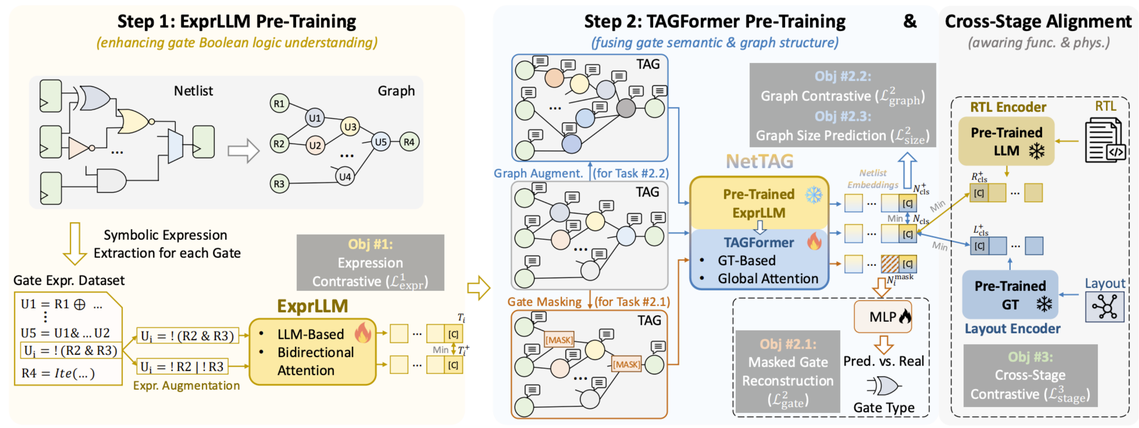
❑ Process: Netlist as Text-Attributed Graph

- **TAG:** gate text semantics (local) + circuit graph structure (global)
  - **Functional:** gate symbolic logic expression
  - **Physical:** gate physical characteristic vector
- **Advantages:**
  - Various gate types &structure independence &LLM compatible



❑ Model: Multimodal Encode & Pre-train

- **Two-phase netlist encoding:** gate text (LLM) + circuit graph (GT)
- **Two-step multimodal pre-training:** functional & physical



Experimental Results

❑ Support Various Largely Different EDA Tasks

- **Functional tasks:** reasoning earlier RTL function (classification)

✓ **Task 1: Comb. gate function**

- Gate-level

Design	GNN-RE [14] Acc. (%)	Prec. (%)	Recall (%)	F1 (%)	NetTAG Acc. (%)	Prec. (%)	Recall (%)	F1 (%)
1	79	82	79	74	97	97	97	97
2	96	96	96	96	100	100	100	100
3	94	94	94	94	100	100	100	100
4	78	83	78	78	100	100	100	100
5	91	92	91	90	99	99	99	99
6	74	78	74	68	94	94	94	93
7	80	80	80	80	84	87	84	81
8	89	90	89	87	95	96	95	96
9	65	77	65	67	100	100	100	100
Avg.	83	86	83	82	**97**	**97**	**97**	**96**

✓ **Task 2: Seq. state/data register**

- Subgraph-level

Design	Task 2 REIGNN [15] Sens. (%)	REIGNN [15] Acc. (%)	NetTAG Sens. (%)	NetTAG Acc. (%)
itc1	50	72	100	98
itc2	100	92	100	100
chipyard1	30	65	80	79
chipyard2	30	65	90	86
vex1	50	74	82	74
vex2	32	60	86	82
opencores1	42	73	93	84
opencores2	37	80	92	82
Avg.	46	73	**90**	**86**

- **Physical tasks:** predicting later layout PPA (regression)

✓ **Task 3: Register slack**

- Subgraph-level

Design	Task 3 GNN* R	GNN* MAPE (%)	NetTAG R	NetTAG MAPE (%)
itc1	0.89	13	0.94	9
itc2	0.91	10	0.93	9
chipyard1	0.72	17	0.7	20
chipyard2	0.86	12	0.95	9
vex1	0.94	11	0.93	12
vex2	0.97	18	0.97	9
opencores1	0.99	26	0.92	29
opencores2	0.93	30	0.98	26
Avg.	0.9	17	**0.92**	**15**

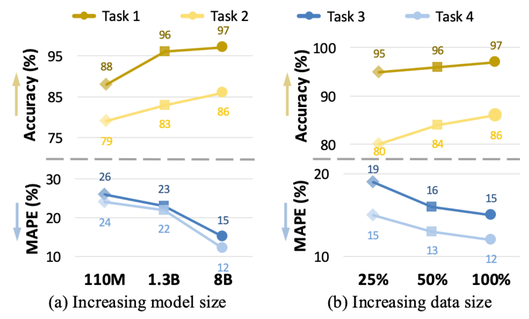
✓ **Task 4: Design power/area**

- Graph-level

Target	Metric†	EDA Tool R	EDA Tool MAPE (%)	GNN* R	GNN* MAPE (%)	NetTAG R	NetTAG MAPE (%)
Area	w/o opt	0.99	5	0.99	5	**0.99**	**4**
	w/ opt	0.95	34	0.95	18	**0.96**	**11**
Power	w/o opt	0.99	34	0.99	12	**0.99**	**8**
	w/ opt	0.73	38	0.76	19	**0.86**	**12**

❑ Circuit Foundation Model Scaling Law

- **Performance scaling up with** model/data size



(a) Increasing model size (b) Increasing data size

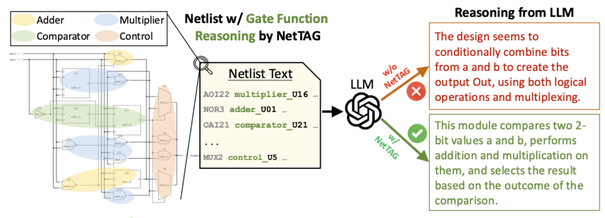
Conclusion and Future Work

❑ NetTAG: Graph-Only → LLM + Graph Fusion

Paper *Code*

❑ Future Work

- Integrate NetTAG into LLMs for generative netlist function reasoning



香港科技大學 THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Contact: wfang838@connect.ust.hk

About me